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Please find below and/or attached an Office communication concerning this application or proceeding.

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 09/981,954 | MEHTA ET AL. | |
| | Examiner | Art Unit | |
| | Kandasamy Thangavelu | 2123 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *19 December 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *1-7,14-21 and 28-45* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-7,14-21 and 28-45* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *18 October 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

## DETAILED ACTION

1. This communication is in response to the Applicants' Amendment dated December 19, 2005. Claims 1, 5-7, 15, 16, 20, 21, 29-31, 35, 37, 38, 40 and 41 were amended. Claims 8-13, 22-27 and 46-49 were canceled. Claims 1-7, 14-21 and 28-45 of the application are pending. This office action is made final.

### *Claim Rejections - 35 USC § 102*

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in-
> (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effect under this subsection of a national application published under section 122(b) only if the international application designating the United States was published under Article 21(2)(a) of such treaty in the English language; or
> (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that a patent shall not be deemed filed in the United States for the purposes of this subsection based on the filing of an international application filed under the treaty defined in section 351(a).

3. Claims 1, 5-7, 14-15, 35-38 and 45 are rejected under 35 U.S.C. § 102(e) as being anticipated by **Djaja et al.** (U.S. Patent 6,405,160).

3.1 **Djaja et al.** teaches Memory compiler interface and methodology. Specifically, as per claim 1, **Djaja et al.** teaches a memory compiler characterization method for determining

parametric data associated with compilable memory instances (Abstract, L1-8; Fig. 2, Item 70; CL1, L5-12; Fig. 4; CL1, L55-57; CL4, L64-67), comprising:

obtaining a first parametric dataset associated with a first plurality of memory compilers, the memory compilers for compiling a first set of memory instances, each instance having a select number of physical rows and a select number of physical columns (Abstract, L1-8; CL1, L31-34; CL2, L16-27; CL5, L13-20), wherein each memory instance is organized using a first MUX factor and further wherein a data point in the first parametric dataset corresponds to a value with respect to a particular parameter characterized for a memory instance sampled from the first set of memory instances (Abstract, L1-8; CL5, L13-20);

obtaining a second parametric dataset by characterizing the particular parameter for a second set of memory instances that are compiled by a second plurality of memory compilers (Abstract, L1-8; Fig. 2, Item 70; CL1, L31-34), each of the second plurality of memory compilers for compiling a respective memory instance organized with a second MUX factor (Abstract, L1-4 and L6-8), wherein the second plurality of memory compilers are sampled from the first plurality of memory compilers such that each memory instance compiled by the second plurality of memory compilers corresponds to a respective congruent memory instance of the first parametric dataset having identical numbers of physical rows and physical columns (Fig. 4, bottom plane at MUX of 2 and top plane at MUX of 16; CL5, L2-12; CL5, L13-20; CL5, L28-31);

determining scale factors for a select number of parametric data points associated with respective congruent memory instances of the first and second parametric datasets (Fig. 4, corner vertical lines; CL2, L46-47; CL4, L64-67; CL5, L52-65);

obtaining an interpolated scale factor based on the scale factors (Fig. 4, the lines defining the horizontal plane in the middle of the cubicle); and

deriving a value of the particular parameter for an additional memory instance having the second MUX factor by applying the interpolated scale factor to a data point associated with a memory instance having the first MUX factor, wherein the memory instance with the first MUX factor is congruent with respect to the additional memory instance with the second MUX factor (Fig. 4, the lines defining the horizontal plane in the middle of the cubicle).

Per claims 5 and 6: **Djaja et al.** teaches that the first MUX factor is selected from at least one of a MUX-4 factor, a MUX-8 factor, a MUX-16 factor and a MUX-32 factor; and the second MUX factor is selected from at least one of a MUX-4 factor, a MUX-8 factor, a MUX-16 factor and a MUX-32 factor (CL5, L28-31; Fig. 4).

Per claim 7: **Djaja et al.** teaches that each memory instance of the first and second sets of memory instances comprises one of a read-only memory (ROM) circuit, a static random access memory (SRAM) circuit, a dynamic random access memory (DRAM) circuit, an electrically programmable ROM (EPROM) circuit, a flash memory circuit, an embedded memory circuit, and a stand-alone memory circuit (CL1, L5-12).

Per claim 14: **Djaja et al.** teaches that the interpolated scale factor is obtained by interpolating four scale factors, each corresponding to a ratio of values of the particular

parameter for a pair of congruent memory instances (Fig. 4, the lines defining the horizontal plane in the middle of the cubicle).

Per claim 15: **Djaja et al.** teaches that the first and second parametric data sets are obtained by characterization of the particular parameter via simulation (Fig. 2, Items 70, 72b; CL2, L10-12; CL5, L47-49).

3.2 As per claim 35, **Djaja et al.** teaches a memory compiler characterization system (Abstract, L1-8; Fig. 2, Item 70; CL1, L5-12; Fig. 4; CL1, L55-57; CL4, L64-67), comprising:

means for characterizing a first plurality of memory compilers with respect to a particular parameter, the first plurality of memory compilers for compiling memory instances of a first type (Abstract, L1-8; CL1, L31-34; CL2, L16-27; CL5, L13-20);

means for characterizing a second plurality of memory compilers with respect to the particular parameter, the second plurality of memory compilers for compiling memory instances of a second type (Abstract, L1-8; Fig. 2, Item 70; CL1, L31-34), wherein the memory instances of second type comprise memory instances sparsely sampled from the memory instances of first type such that each sampled memory instance of second type corresponds to a respective congruent memory instance of first type having identical numbers of physical rows and physical columns (Fig. 4, bottom plane at MUX of 2 and top plane at MUX of 16; CL5, L2-12; CL5, L13-20; CL5, L28-31);

means for determining scale factors between values of the particular parameter respectively associated with a pair of congruent memory instances of the first and second types (Fig. 4, corner vertical lines; CL2, L46-47; CL4, L64-67; CL5, L52-65);

an interpolator to obtain an interpolated scale factor based on the scale factors (Fig. 4, the lines defining the horizontal plane in the middle of the cubicle); and

means for obtaining a value of the particular parameter for an additional memory instance of second type by utilizing the interpolated scale factor in conjunction with a parametric value of a congruent memory instance of first type which corresponds to the additional memory instance (Fig. 4, the lines defining the horizontal plane in the middle of the cubicle).

Per claims 36, 37 and 38: **Djaja et al.** teaches that the memory instances of first type comprise memory instances with a first MUX factor and the memory instances of second type comprise memory instances with a second MUX factor; the first MUX factor is selected from at least one of a MUX-4 factor, a MUX-8 factor, a MUX-26 factor and a MUX-32 factor; and the second MUX factor is selected from at least one of a MUX-4 factor, a MUX-8 factor, a MUX-7.6 factor and a MUX-32 factor (CL5, L28-31; Fig. 4).

Per claim 45: **Djaja et al.** teaches that the memory instances comprise one of a DRAM circuit, an SRAM circuit, a ROM circuit, an EPROM circuit and a flash memory circuit (CL1, L5-12).

## *Claim Rejections - 35 USC § 103*

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains.

5. The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

6. Claims 2-4 are rejected under 35 U.S.C. 103(a) as being unpatentable over **Djaja et al.** (U.S. Patent 6,405,160) in view of **Yuan et al.** (U.S. Patent 6,249,901).

6.1 As per claim 2, **Djaja et al.** teaches the method of claim 1. **Djaja et al.** does not expressly teach that the particular parameter comprises a memory timing parameter. **Yuan et al.** teaches that the particular parameter comprises a memory timing parameter (Abstract, L1-3 and L7-11; Fig. 3; Fig. 5, Items 214, 236 and 244; Fig. 6B, Items 272, 290; Fig. 6D, Items 272, 304, 310 and 312; CL2, L8-35), because that allows the IC designers to optimize the memory timing

parameters to increase the performance of the memory circuit (CL2, L5-7; CL5, L37-39); and the memory characterization method provides improved accuracy in determining the timing characteristics and generates a large number of memory instances of a memory compiler in a relatively short period of time (CL5, L65-67; CL6, L58-62). It would have been obvious to one of ordinary skill in the art at the time of Applicants' invention to modify the method of **Djaja et al.** with the method of **Yuan et al.** that included the particular parameter comprising a memory timing parameter. The artisan would have been motivated because that would allow the IC designers to optimize the memory timing parameters to increase the performance of the memory circuit; and the memory characterization method would provide improved accuracy in determining the timing characteristics and generate a large number of memory instances of a memory compiler in a relatively short period of time.

6.2 As per claims 3 and 4, **Djaja et al.** and **Yuan et al.** teach the method of claim 2. **Djaja et al.** does not expressly teach that the memory timing parameter comprises memory access time; and the memory timing parameter comprises memory cycle time. **Yuan et al.** teaches that the memory timing parameter comprises memory access time; and the memory timing parameter comprises memory cycle time (CL1, L66 to CL2, L5), because that allows the IC designers to optimize the memory timing parameters to increase the performance of the memory circuit (CL2, L5-7; CL5, L37-39); and the memory characterization method provides improved accuracy in determining the timing characteristics and generates a large number of memory instances of a memory compiler in a relatively short period of time (CL5, L65-67; CL6, L58-62). It would have been obvious to one of ordinary skill in the art at the time of Applicants' invention to

modify the method of **Djaja et al.** with the method of **Yuan et al.** that included the memory timing parameter comprising memory access time; and the memory timing parameter comprising memory cycle time. The artisan would have been motivated because that would allow the IC designers to optimize the memory timing parameters to increase the performance of the memory circuit; and the memory characterization method would provide improved accuracy in determining the timing characteristics and generate a large number of memory instances of a memory compiler in a relatively short period of time.

7. Claims 16, 20-21, 28-34 and 39-44 are rejected under 35 U.S.C. 103(a) as being unpatentable over **Djaja et al.** (U.S. Patent 6,405,160) in view of **Murotani** (U.S. Patent 5,175,707).

7.1 As per claim 16, **Djaja et al.** teaches a memory compiler characterization method for determining parametric data associated with compilable memory instances (Abstract, L1-8; Fig. 2, Item 70; CL1, L5-12; Fig. 4; CL1, L55-57; CL4, L64-67), comprising:

obtaining a first parametric dataset associated with a first plurality of memory compilers, each of the memory compilers for compiling a respective memory instance having a select number of physical rows and a select number of physical columns (Abstract, L1-8; CL1, L31-34; CL2, L16-27; CL5, L13-20), and organized using a select MUX factor wherein a data point in the first parametric dataset corresponds to a value with respect to a particular parameter characterized for a memory instance sampled from the first set of memory instances (Abstract, L1-8; CL5, L13-20);

obtaining a second parametric dataset by characterizing the particular parameter for a second set of memory instances compiled by a second plurality of memory compilers (Abstract, L1-8; Fig. 2, Item 70; CL1, L31-34), each of the second plurality of memory compilers for compiling a respective memory instance organized with a second MUX factor (Abstract, L1-4 and L6-8), wherein the second plurality of memory compilers are sampled from the first plurality of memory compilers such that each memory instance compiled by the second plurality of memory compilers corresponds to a respective congruent memory instance of the first parametric dataset having identical numbers of physical rows and physical columns (Fig. 4, bottom plane at MUX of 2 and top plane at MUX of 16; CL5, L2-12; CL5, L13-20; CL5, L28-31);

determining scale factors for a select number of parametric data points associated with respective congruent memory instances of the first and second parametric datasets (Fig. 4, corner vertical lines; CL2, L46-47; CL4, L64-67; CL5, L52-65);

obtaining an interpolated scale factor based on the scale factors (Fig. 4, the lines defining the horizontal plane in the middle of the cubicle); and

deriving a value of the particular parameter for an additional memory instance of second parametric dataset by applying the interpolated scale factor to a data point associated with a memory instance of the first parametric dataset, wherein the memory instance is congruent with respect to the additional memory instance of the second parametric dataset (Fig. 4, the lines defining the horizontal plane in the middle of the cubicle).

**Djaja et al.** does not expressly teach that the first plurality of memory compilers are representative of a first memory technology; the second plurality of memory compilers are

representative of a second memory technology; and deriving a value of the particular parameter for an additional memory instance of the second memory technology by applying the interpolated scale factor to a data point associated with a memory instance of the first memory technology, wherein the memory instance of the first memory technology is congruent with respect to the additional memory instance of the second memory technology. **Murotani** teaches that the first plurality of memory compilers are representative of a first memory technology; the second plurality of memory compilers are representative of a second memory technology; and deriving a value of the particular parameter for an additional memory instance of the second memory technology by applying the interpolated scale factor to a data point associated with a memory instance of the first memory technology, wherein the memory instance of the first memory technology is congruent with respect to the additional memory instance of the second memory technology (CL1, L20-26. It would have been obvious to one of ordinary skill in the art at the time of Applicants' invention to modify the method of **Djaja et al.** with the method of **Murotani** that included the first plurality of memory compilers being representative of a first memory technology; the second plurality of memory compilers are representative of a second memory technology; and deriving a value of the particular parameter for an additional memory instance of the second memory technology by applying the interpolated scale factor to a data point associated with a memory instance of the first memory technology, wherein the memory instance of the first memory technology is congruent with respect to the additional memory instance of the second memory technology because the memory technology selected would depend on the size and capacity of the memory required for the application (CL1, L20-26).

Per claim 20: **Djaja et al.** teaches that the select MUX factor is selected from at least one of a MUX-4 factor, a MUX-8 factor, a MUX-16 factor and a MUX-32 factor (CL5, L28-31; Fig. 4).

Per claim 21: **Djaja et al.** teaches that each memory instance of the first and second sets of memory instances comprises one of a read-only memory (ROM) circuit, a static random access memory (SRAM) circuit, a dynamic random access memory (DRAM) circuit, an electrically programmable ROM (EPROM) circuit, a flash memory circuit, an embedded memory circuit, and a stand-alone memory circuit (CL1, L5-12).

Per claim 28: **Djaja et al.** teaches that the interpolated scale factor is obtained by interpolating four scale factors, each corresponding to a ratio of values of the particular parameter for a pair of congruent memory instances (Fig. 4, the lines defining the horizontal plane in the middle of the cubicle).

Per claim 29: **Djaja et al.** teaches that the first and second parametric datasets are obtained by characterization of the particular parameter via simulation n (Fig. 2, Items 70, 72b; CL2, L10-12; CL5, L47-49).

7.2 As per claims 30 and 31, **Djaja et al.** and **Murotani** teach the method of claim 16. **Djaja et al.** does not expressly teach that the first memory technology is selected from at least one of 1.0 μ technology, 0.8 μ technology, 0.6 μ technology and 0.2 μ technology; and the second

memory technology is selected from at least one of 1.0 μ technology, 0.8 μ technology, 0.6 μ technology and 0.2 μ technology. **Murotani** teaches that the first memory technology is selected from at least one of 1.0 μ technology, 0.8 μ technology, 0.6 μ technology and 0.2 μ technology; and the second memory technology is selected from at least one of 1.0 μ technology, 0.8 μ technology, 0.6 μ technology and 0.2 μ technology (CL1, L20-26). It would have been obvious to one of ordinary skill in the art at the time of Applicants' invention to modify the method of **Djaja et al.** with the method of **Murotani** that included the first memory technology being selected from at least one of 1.0 μ technology, 0.8 μ technology, 0.6 μ technology and 0.2 μ technology; and the second memory technology being selected from at least one of 1.0 μ technology, 0.8 μ technology, 0.6 μ technology and 0.2 μ technology because the memory technology selected would depend on the size and capacity of the memory required for the application (CL1, L20-26).

7.3 As per claim 32, **Djaja et al.** and **Murotani** teach the method of claim 16. **Djaja et al.** does not expressly teach that the first and second memory technologies comprise design rule-specific technologies. **Murotani** teaches that the first and second memory technologies comprise design rule-specific technologies (CL1, L20-26), because the memory technology selected depends on the size and capacity of the memory required for the application (CL1, L20-26). It would have been obvious to one of ordinary skill in the art at the time of Applicants' invention to modify the method of **Djaja et al.** with the method of **Murotani** that included the first and second memory technologies comprising design rule-specific technologies. The artisan

would have been motivated because the memory technology selected would depend on the size and capacity of the memory required for the application.

Per claims 33 and 34: **Djaja et al.** teaches that the first and second memory technologies comprise foundry specific technologies; and the first and second memory technologies comprise process flow-specific technologies (CL2, L16-19).

7.4 As per claim 39, **Djaja et al.** teaches the system of claim 35. **Djaja et al.** does not expressly teach that the memory instances of first type comprise memory instances associated with a first memory technology and the memory instances of second type comprise memory instances associated with a second memory technology. **Murotani** teaches that the memory instances of first type comprise memory instances associated with a first memory technology and the memory instances of second type comprise memory instances associated with a second memory technology (CL1, L20-26), because the memory technology selected depends on the size and capacity of the memory required for the application (CL1, L20-26). It would have been obvious to one of ordinary skill in the art at the time of Applicants' invention to modify the system of **Djaja et al.** with the system of **Murotani** that included the memory instances of first type comprising memory instances associated with a first memory technology and the memory instances of second type comprising memory instances associated with a second memory technology. The artisan would have been motivated because the memory technology selected would depend on the size and capacity of the memory required for the application.

7.5 As per claims 40 and 41, **Djaja et al.** and **Murotani** teach the system of claim 39. **Djaja et al.** does not expressly teach that the first memory technology is selected from at least one of 1.0 μ technology, 0.8 μ technology, 0.6 μ technology and 0.2 μ technology; and the second memory technology is selected from at least one of 1.0 μ technology, 0.8 μ technology, 0.6 μ technology and 0.2 μ technology. **Murotani** teaches that the first memory technology is selected from at least one of 1.0 μ technology, 0.8 μ technology, 0.6 μ technology and 0.2 μ technology; and the second memory technology is selected from at least one of 1.0 μ technology, 0.8 μ technology, 0.6 μ technology and 0.2 μ technology (CL1, L20-26). It would have been obvious to one of ordinary skill in the art at the time of Applicants' invention to modify the system of **Djaja et al.** with the system of **Murotani** that included the first memory technology being selected from at least one of 1.0 μ technology, 0.8 μ technology, 0.6 μ technology and 0.2 μ technology; and the second memory technology being selected from at least one of 1.0 μ technology, 0.8 μ technology, 0.6 μ technology and 0.2 μ technology because the memory technology selected would depend on the size and capacity of the memory required for the application (CL1, L20-26).

7.6 As per claim 42, **Djaja et al.** and **Murotani** teach the system of claim 35. **Djaja et al.** does not expressly teach that the first and second memory technologies comprise design rule-specific technologies. **Murotani** teaches that the first and second memory technologies comprise design rule-specific technologies (CL1, L20-26), because the memory technology selected depends on the size and capacity of the memory required for the application (CL1, L20-26). It would have been obvious to one of ordinary skill in the art at the time of Applicants'

invention to modify the system of **Djaja et al.** with the system of **Murotani** that included the first and second memory technologies comprising design rule-specific technologies. The artisan would have been motivated because the memory technology selected would depend on the size and capacity of the memory required for the application.

Per claims 43 and 44: **Djaja et al.** teaches that the first and second memory technologies comprise foundry specific technologies; and the first and second memory technologies comprise process flow-specific technologies (CL2, L16-19).

8. Claims 17-19 are rejected under 35 U.S.C. 103(a) as being unpatentable over **Djaja et al.** (U.S. Patent 6,405,160) in view of **Murotani** (U.S. Patent 5,175,707), and further in view of **Yuan et al.** (U.S. Patent 6,249,901).

8.1 As per claim 17, **Djaja et al.** and **Murotani** teach the method of claim 16. **Djaja et al.** does not expressly teach that the particular parameter comprises a memory timing parameter. **Yuan et al.** teaches that the particular parameter comprises a memory timing parameter (Abstract, L1-3 and L7-11; Fig. 3; Fig. 5, Items 214, 236 and 244; Fig. 6B, Items 272, 290; Fig. 6D, Items 272, 304, 310 and 312; CL2, L8-35), because that allows the IC designers to optimize the memory timing parameters to increase the performance of the memory circuit (CL2, L5-7; CL5, L37-39); and the memory characterization method provides improved accuracy in determining the timing characteristics and generates a large number of memory instances of a memory compiler in a relatively short period of time (CL5, L65-67; CL6, L58-62). It would

have been obvious to one of ordinary skill in the art at the time of Applicants' invention to modify the method of **Djaja et al.** with the method of **Yuan et al.** that included the particular parameter comprising a memory timing parameter. The artisan would have been motivated because that would allow the IC designers to optimize the memory timing parameters to increase the performance of the memory circuit; and the memory characterization method would provide improved accuracy in determining the timing characteristics and generate a large number of memory instances of a memory compiler in a relatively short period of time.

8.2 As per claims 18 and 19, **Djaja et al., Murotani** and **Yuan et al.** teach the method of claim 2. **Djaja et al.** does not expressly teach that the memory timing parameter comprises memory access time; and the memory timing parameter comprises memory cycle time. **Yuan et al.** teaches that the memory timing parameter comprises memory access time; and the memory timing parameter comprises memory cycle time (CL1, L66 to CL2, L5), because that allows the IC designers to optimize the memory timing parameters to increase the performance of the memory circuit (CL2, L5-7; CL5, L37-39); and the memory characterization method provides improved accuracy in determining the timing characteristics and generates a large number of memory instances of a memory compiler in a relatively short period of time (CL5, L65-67; CL6, L58-62). It would have been obvious to one of ordinary skill in the art at the time of Applicants' invention to modify the method of **Djaja et al.** with the method of **Yuan et al.** that included the memory timing parameter comprising memory access time; and the memory timing parameter comprising memory cycle time. The artisan would have been motivated because that would allow the IC designers to optimize the memory timing parameters to increase the performance of

the memory circuit; and the memory characterization method would provide improved accuracy in determining the timing characteristics and generate a large number of memory instances of a memory compiler in a relatively short period of time.

## *Response to Arguments*

9. Applicants' arguments with respect to 35 USC 102 (e) and 35 USC 103 (a) rejections filed on December 19, 2005 have been considered. Applicants' arguments with respect to 35 USC 102 (e) and 35 USC 103 (a) rejections are not persuasive.

9.1 As per the applicants' argument that, "each data point in said first parametric dataset corresponds to a value with respect to a particular parameter characterized for a memory instance sampled from all possible memory configurations (i.e., varying number of rows and varying number of columns) comprising the first set of memory instances; a second parametric dataset is obtained by characterizing the same parameter for a second set of memory instances that are compiled by a second plurality of memory compilers, but with a second MUX factor; the second plurality of memory compilers are sampled from the first plurality of memory compilers, in that not all memory configurations that were characterized in the first parametric dataset are characterized for the second parametric dataset; ... the memory instances of second type comprise memory instances sparsely sampled from the memory instances of first type such that each sampled memory instance of second type corresponds to a respective congruent memory instance of first type having identical numbers of physical rows and physical columns; ... the

**Djaja** reference requires simulation of all possible memory configurations (i.e. matrix combinations of bits per word, number of rows and column MUX factor) for purposes of determining the characteristic equations; to the extent the database corresponding to two different levels (e.g., the bottom plane at MUX 2 and the top plane at MUX 16) of Fig. 4 of the **Djaja** reference, it can be equated to the first and second parametric data sets as claimed by the applicant; the second parametric dataset is not obtained as a sparsely sampled set of data points with respect to the first parametric dataset since the datasets at MUX 2 and MUX 16 in the **Djaja** are co-extensive; for each data point determined at MUX 2 level, there is a corresponding data point determined at MUX 16 level as well", the Examiner takes the position that the **Djaja** reference uses four point interpolation as used by the applicant. Therefore it performs simulations at the congruent points in the first parametric dataset and the second parametric dataset as performed by the applicant. While the applicant claims that "the second parametric dataset is obtained as a sparsely sampled set of data points with respect to the first parametric dataset", in reality he does the simulations at all points that are required for the four point interpolation as done by the **Djaja** reference. The Examiner does not see any difference between the method of **Djaja** reference and the applicant's method.

**Djaja et al.** teaches obtaining a first parametric dataset associated with a first plurality of memory compilers, the memory compilers for compiling a first set of memory instances, each instance having a select number of physical rows and a select number of physical columns (Abstract, L1-8; CL1, L31-34; CL2, L16-27; CL5, L13-20), wherein each memory instance is organized using a first MUX factor and further wherein a data point in the first parametric

dataset corresponds to a value with respect to a particular parameter characterized for a memory instance sampled from the first set of memory instances (Abstract, L1-8; CL5, L13-20);

obtaining a second parametric dataset by characterizing the particular parameter for a second set of memory instances that are compiled by a second plurality of memory compilers (Abstract, L1-8; Fig. 2, Item 70; CL1, L31-34), each of the second plurality of memory compilers for compiling a respective memory instance organized with a second MUX factor (Abstract, L1-4 and L6-8), wherein the second plurality of memory compilers are sampled from the first plurality of memory compilers such that each memory instance compiled by the second plurality of memory compilers corresponds to a respective congruent memory instance of the first parametric dataset having identical numbers of physical rows and physical columns (Fig. 4, bottom plane at MUX of 2 and top plane at MUX of 16; CL5, L2-12; CL5, L13-20; CL5, L28-31).

**Djaja et al.** teaches means for characterizing a first plurality of memory compilers with respect to a particular parameter, the first plurality of memory compilers for compiling memory instances of a first type (Abstract, L1-8; CL1, L31-34; CL2, L16-27; CL5, L13-20);

means for characterizing a second plurality of memory compilers with respect to the particular parameter, the second plurality of memory compilers for compiling memory instances of a second type (Abstract, L1-8; Fig. 2, Item 70; CL1, L31-34), wherein the memory instances of second type comprise memory instances sparsely sampled from the memory instances of first type such that each sampled memory instance of second type corresponds to a respective congruent memory instance of first type having identical numbers of physical rows and physical

columns (Fig. 4, bottom plane at MUX of 2 and top plane at MUX of 16; CL5, L2-12; CL5, L13-20; CL5, L28-31).

9.2 As per the applicants' argument that, "the critical deficiencies of the **Djaja** reference as applied are not cured by the secondary references, i.e., the Yuan and Murotani references, either individually or in combination, when used as a basis for obviousness; the combined teachings of the applied art do not teach or suggest all limitations as currently recited at least as to: (i) obtaining a first parametric dataset associated with a first plurality of memory compilers, wherein a data point corresponds to a value with respect to a particular parameter characterized for a memory instance sampled from all possible memory configurations; and (ii) obtaining a second parametric dataset by characterizing the same parameter for a second set of memory instances that are compiled by a second plurality of memory compilers, wherein the second plurality of memory compilers are sampled from the first plurality of memory compilers in that not all memory configurations that were characterized in the first parametric dataset are characterized for the second parametric dataset", the Examiner takes the position that as explained in Paragraph 9.1 above, **Djaja** reference uses four point interpolation as used by the applicant. Therefore it performs simulations at the congruent points in the first parametric dataset and the second parametric dataset as performed by the applicant. While the applicant claims that "the second parametric dataset is obtained as a sparsely sampled set of data points with respect to the first parametric dataset", in reality he does the simulations at all points that are required for the four point interpolation as done by the **Djaja** reference. The Examiner does not see any difference between the method of **Djaja** reference and the applicant's method.

## *Conclusion*

## *ACTION IS FINAL*

10. Applicant's arguments with respect to claim rejections under 35 USC § 103 (a) are not persuasive. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

11. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Dr. Kandasamy Thangavelu whose telephone number is 571-272-3717. The examiner can normally be reached on Monday through Friday from 8:00 AM to 5:30 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Leo Picard, can be reached on 571-272-3749. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to TC 2100 Group receptionist: 571-272-2100.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

K. Thangavelu
Art Unit 2123
January 14, 2006

Paul L. Rodriguez 1/15/06
Primary Examiner
Art Unit 2125